We CLAIM:

1. The method of fabricating a backside surface for a wafer of microwave radio frequency circuit die, said method comprising the steps of:

SUB A3

forming an array of front side via holes of selected location and depth dimension in said wafer of circuit die;

said step of forming an array of via holes being performed during a front side accessing of said wafer of circuit die;

disposing a grid pattern mask on said backside surface of said wafer of microwave radio frequency circuit die;

said grid pattern mask including a backside periphery outline masking for each circuit die of said wafer;

removing a layer of selected thickness from said wafer backside surface, said removing being from exposed backside surface areas intermediate said grid pattern masking;

said removing step leaving recessed valley portions of selected thickness disposed intermediate individual circuit die-strengthening upstanding surrounding bluff masked regions in said wafer backside surface.

2. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said wafer has an initial overall thickness between five hundred and six hundred twenty five micrometers and has a final thickness of between twenty five and one hundred micrometers in said removed layer recessed valley portions.

3. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said step of forming an array of via holes is performed during one of before fabrication of said microwave radio frequency circuit on said die and after fabrication of said microwave radio frequency circuit on said die.

4. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 1 further including the step of forming an etching depth vernier marker pattern in each die backside surface of said wafer after said step of forming an array of front side via holes.

5. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said backside periphery outline masking is disposed in a closed geometric pattern encircling each front side microwave radio frequency circuit die and further including a closed geometric pattern backside annular ring of original wafer thickness semiconductor material surrounding said entire wafer of microwave radio frequency circuit die.

6. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said step of removing a layer of selected thickness from said wafer backside surface includes a backside surface etching step.

7. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 6 wherein said backside surface etching step comprises a dry gas etching sequence.

8. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 7 wherein said backside surface etching step includes one of an inductively coupled plasma and an electron cyclotron resonance fast etching processes.

9. The method of fabricating a circuit-free backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said removing step individual circuit die-strengthening upstanding surrounding bluff masked regions further include a wafer periphery-surrounding annular ring upstanding bluff region.

10. Radio frequency circuit die apparatus comprising the combination of:

a semiconductor wafer having a plurality of individual radio frequency electrical circuit devices received in individual die locations across a frontal surface thereof;

an array of recessed cavity regions disposed across a backside surface of said semiconductor wafer;

each said recessed cavity region of said backside array being disposed in lateral registration with one of said frontal surface radio frequency electrical circuit die locations and comprising a region of diminished wafer thickness and enhanced electrical and thermal performance for components of said registered frontal surface radio frequency electrical circuit device;

SUB A3

each said recessed cavity region in said backside array being bounded by a pattern of plateau cross-sectioned wafer material disposed in both lateral registration with a periphery of each said circuit die and in rigidifying physical strengthening of said circuit die and said region of diminished semiconductor wafer thickness.

11. The radio frequency circuit die apparatus of claim 10 wherein each said recessed cavity region has a depth in excess of four hundred microns and said circuit die has a remaining thickness less than one hundred microns at said recessed cavity region.

12. The radio frequency circuit die apparatus of claim 10 wherein said pattern of plateau cross-sectioned wafer material is configured in the form of a waffle-like interconnected grid disposed across said wafer backside surface.

13. The radio frequency circuit die apparatus of claim 10 further including an array of via holes dispersed across said wafer as a selected number of holes for each said radio frequency electrical circuit device.

14. The radio frequency circuit die apparatus of claim 13 wherein said via holes have a first larger diameter at said wafer frontal surface and a smaller second diameter at said wafer backside surface.

15. The radio frequency circuit die apparatus of claim 13 further including a layer of metal received in each said via hole and disposed in electrical interconnection continuity with first layer metal located on said wafer frontal surface and second layer ground plane metal disposed over said wafer backside surface.

16. The radio frequency circuit die apparatus of claim 13 wherein each said via hole is surrounded by a region of electrically insulating wafer semiconductor material.

17. The radio frequency circuit die apparatus of claim 13 wherein said circuit die has a remaining thickness at said recessed cavity region equal to a depth dimension of said via holes.

18. The radio frequency circuit die apparatus of claim 10 wherein said pattern of plateau cross-sectioned wafer material includes a mask material first metal layer and a ground plane material second metal layer covering a plateau surface portion of said plateau cross-sectioned wafer material.

SUB A3

19. The radio frequency circuit die apparatus of claim 10 wherein said radio frequency electrical circuit devices are microwave monolithic integrated circuit devices.

20. The radio frequency circuit die apparatus of claim 13 further including a multiple pointed vernier marker etch depth indicator element disposed adjacent selected of said via holes in said semiconductor wafer.

21. The radio frequency circuit die apparatus of claim 10 wherein said pattern of plateau cross-sectioned wafer material includes an upstanding surrounding perimeter of plateau cross-sectioned wafer material.

22. The method of making a thinned semiconductor wafer radio frequency integrated circuit device of damage resistant physical integrity, desirable high frequency electrical characteristics and favorable thermal energy dissipating characteristics, said method comprising the steps of:

fabricating electrical circuit portions of said thinned semiconductor wafer radio frequency integrated circuit device on a frontal side of a nominal thickness semiconductor wafer, each said integrated circuit device being disposed in a separate die location of said semiconductor wafer and including a plurality of contact pads;

forming a plurality of via hole intrusions into said nominal thickness semiconductor wafer in locations registered with selected of said contact pads of said integrated circuit device;

said via hole intrusions being formed from said frontal side of said nominal thickness semiconductor wafer and having a first diameter adjacent said wafer frontal side and a second smaller diameter within a thickness portion of said wafer;

metallizing said via hole openings, said metallizing including establishing via metal electrical connections with selected of said contact pads;

depositing a mask of grid pattern-defining configuration on said wafer backside surface;

said mask of grid pattern-defining configuration determining a plurality of wafer backside grid cells each aligned in surrounding periphery with one of said wafer frontal surface integrated circuit devices;

removing a controlled thickness amount of semiconductor wafer backside surface semiconductor material within each said backside grid cell, said removing including an etching

step and leaving a wafer backside grid pattern of semiconductor material of said semiconductor wafer nominal thickness dimension and leaving a selected thickness remainder amount of said semiconductor wafer nominal thickness dimension material, within each said backside grid cell, in support of each said integrated circuit device;

said etching step also leaving a wafer perimeter-disposed backside ring of wafer semiconductor material of said semiconductor wafer nominal thickness dimension and integral interconnection with said wafer backside grid pattern of wafer nominal thickness dimension;

said wafer perimeter-disposed backside ring of wafer semiconductor material of said semiconductor wafer nominal thickness dimension and said wafer backside grid pattern of wafer nominal thickness dimension semiconductor material in interconnecting combination adding physical handling-assisting substantial physical integrity and rigidity to said now thinned semiconductor wafer;

covering said thinned semiconductor wafer backside including said wafer backside grid pattern cells with a layer of ground plane metal, said covering including forming ground plane electrical interconnections with said via hole intrusions metallization;

mounting said wafer on said frontal surface thereof;

further processing said wafer during continued frontal surface mounting, said further processing including removing each integrated circuit device die from said wafer by wafer segregation within a lateral extent of a backside grid cell.

23. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said step of forming a plurality of via hole intrusions into said semiconductor wafer includes:

disposing said via hole intrusions to a first depth dimension into said semiconductor wafer; and

wherein said selected thickness remainder amount of said semiconductor wafer nominal thickness dimension material in said step of removing a controlled thickness amount of said wafer backside semiconductor material within each said backside grid cell comprises leaving a selected thickness remainder amount of said wafer nominal thickness equal to said via hole intrusions first depth dimension into said semiconductor wafer.

SUB A37

24. The method of making a thinned wafer radio frequency integrated circuit device of claim 23 wherein:

said semiconductor wafer of nominal thickness is between five hundred and six hundred twenty-five micrometers in thickness; and

wherein said selected thickness remainder amount of said wafer nominal thickness and said via hole intrusions first depth dimension are each no more than one hundred micrometers.

25. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said radio frequency integrated circuit device is comprised of one of field effect and bipolar junction and heterojunction bipolar transistors.

26. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said desirable high frequency electrical characteristics include thin substrate-controlling electrical inductances within said integrated circuit device.

27. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said depositing step mask is a metallic mask.

28. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said removing step etching comprises an anisotropic etching, dry gas, reactive ion, plasma etching sequence.

29. The method of making a thinned wafer radio frequency integrated circuit device of claim 28 wherein said anisotropic etching, dry gas, reactive ion, plasma etching sequence comprises one of an inductively coupled plasma (ICP) and an electron cyclotron resonance (ECR) high density plasma etching sequences.

30. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said covering step forming of ground plane electrical interconnections comprises covering underside portions of etching-exposed second smaller diameter via hole metallizations with ground plane metal.